Integrated 48 GHz LO Chain for 60 GHz Communication Systems

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***Abstract*— A frequency doubler with pre-amplifier and driver amplifier for the LO chain of a 60 GHz communication system has been designed and tested. The circuit has been designed in conjunction with other transceiver sub-systems in the 0.15 µm GaAs pHEMT process of UMS (PH15). The measurements show good fundamental suppression of 35 dBc and an output power that can drive the co-designed mixer circuit. The doubler chain with amplifiers is approx. 3x1.3 mm, has a gain of 11 dB and a P_{-1dB} at the output of +11 dBm.**

I. Introduction

High data rate communication requires sufficient bandwidth or large signal to noise ratios. Especially in currently appointed frequency bands for wireless communication the growing number of systems and wide spread use of these systems sets a limit on the signal to noise ratio achievable. To solve this basically two solutions are pursued: ultra-wide band in the band from 3 to 10 GHz and a part of the frequency spectrum around 60 GHz with a large continuous bandwidth. The use of the latter frequency band is not subject to licenses, only restrictions apply to the radiated power (standardisation is currently under discussion [1]).

Communication systems for the 60 GHz band require high-frequency local oscillator (LO) signals with small spurious signals. The transceiver chip set envisaged requires a 48 GHz LO signal. This cannot be supplied directly and therefore a doubler circuit has been added to the LO chain.

This MMIC is part of a chip set that is developed for short range high data rate communications in the 60 GHz band. In the same run also a low-noise amplifier (LNA), mixer, driver amplifier and filter, as well as two complete transmit and receive MMICs are designed. They will be reported separately.

II. Design

We selected the 0.15 µm GaAs pHEMT process of UMS, PH15. This choice has been driven mostly by the required noise figure and output power for other circuits in the same chipset.

The IF frequency and LO frequency have been selected such that little of the low-order spurious products (up to fifth order) lie in-band. An IF around 13 GHz and an LO at 48 GHz has been selected. The doubler output signal should not contain high levels of the fundamental frequency. These will generate spurious components in-band. Therefore a doubler architecture has been chosen that inherently suppresses the fundamental signal. Two FETs in parallel are driven with equal signals but with 180° phase difference. The outputs are combined in the matching network. The fundamental signal will cancel in the output due to the phase difference. The double frequency however has relative phase of twice 180° and will add in-phase. At the input of the doubler a circuit has been used to generate equal but out-of-phase signals. This is done with a ratrace. The size of a ratrace at 24 GHz made with standard λ/4 lines (1200 µm) is too large for integration on GaAs. A semi-lumped equivalent is used instead.

The mixer in the transmit chain has to have a high output power compression point to prevent a large gain requirement at 60 GHz in the driver, which cannot be efficiently obtained at these frequencies. This requirement dictates a relatively high LO power at the mixer port. From preliminary mixer simulations it was observed that the mixer conversion loss did not increase when the LO power was at least 11.5 dBm. This level could not be obtained directly for the doubler, a 48 GHz amplifier stage is added at the output. Two amplifier stages are added at the input of the circuit to be able to connect the LO chain to a source of 0 dBm at 24 GHz. As ample gain is available at the design frequency of 24 GHz the first stage is stabilised by an RC feedback. The next stage is a compromise between gain and the required drive power for the doubler. These stages are made with 2x30 µm and 4x60 µm FETs respectively. The devices in the doubler are 6x35 µm FETs and the output driver is a 4x45 µm FET.

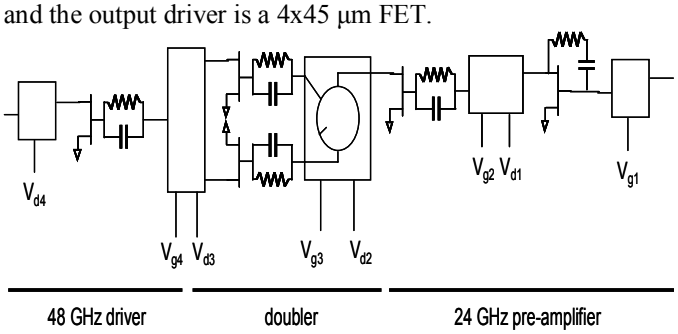

Fig. 1 Architecture of the doubler with peripheral amplifiers. Signal flow is from right to left to match the photo in Fig. 2.

The DC connections will all be on one side of the MMIC as the device is meant for integration in a transceiver MMIC and only one side of the part can lie along an outer edge.

III. Simulations

The core of the doubler, two FETs near pinch off, driven in anti-phase are fed from a ratrace circuit. The ratrace at 24 GHz, when made from λ/4 lines, would have a diameter of 1500 µm. The λ/4 line have therefore been synthesised from high-impedance lines and capacitors in a π-network. By lowering the characteristic impedance of these lines the structure became even smaller. The chosen impedance of 25 Ω was the lowest possible with the capacitor size available in the process library, 0.2 pF. The ratrace is only 450x800 µm and has good amplitude and phase characteristics. The bandwidth for 5% phase deviation from 180° is 19.1 to 25.5 GHz and for 0.5 dB amplitude variation is 21.7 to 24.9 GHz.

The output power of the double frequency can be tuned with the gate bias of the doubler FETs. Gate voltages of -03. to -0.7 V result in output powers of 10 to 13 dBm. A suppression of the fundamental frequency of more than 50 dB with respect to the double frequency output power has been simulated.

IV. Measurements

The circuits have been delivered on a 4" wafer of 100 µm thick. All measurements have been performed on-wafer with GGB picoprobes and DC needles with capacitors of 120 pF on the thicker end of the needles, about 10 mm away from the probe tips. These have been added for stability improvement at low frequencies. The calibration for the RF path has been done with the TRL method [2].

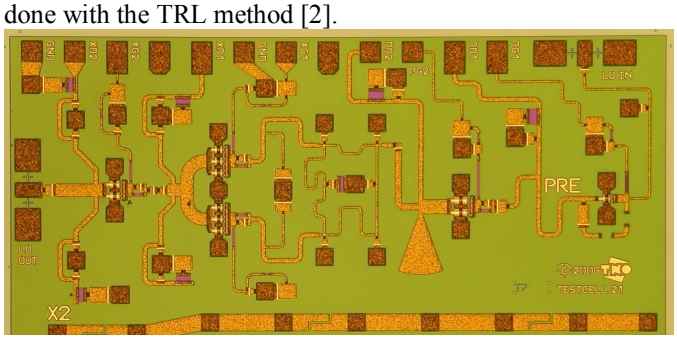

Fig. 2 Photo of the preamplifier, doubler and 48 GHz driver.

Apart from the complete doubler chain with amplifiers also test structures of the pre-amplifier (2 stages at 24 GHz), 24 GHz ratrace (3-port structure) and doubler plus output amplifier have been included on the wafer and measured.

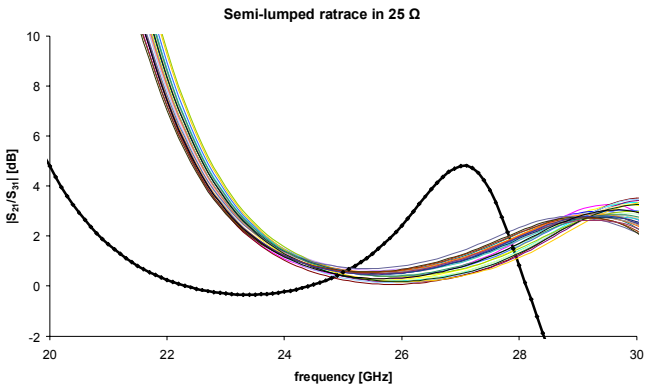

Fig. 3 Comparison of measured (thin curves) and simulated (thick curve) amplitude difference between the output ports of the ratrace.

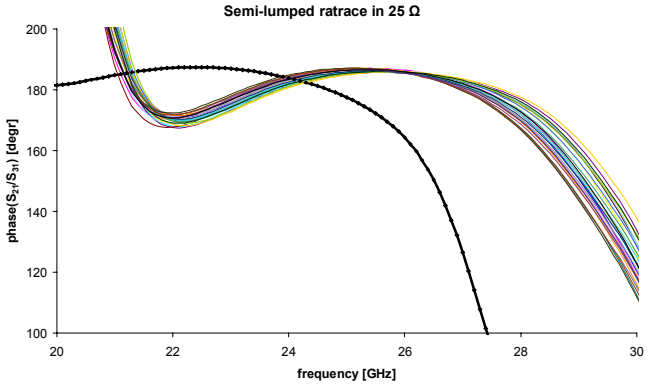

Fig. 4 Comparison of measured (thin curves) and simulated (thick curve) phase difference between the output ports of the ratrace.

Stability has been checked and extra decoupling for around 1 GHz has to be added on the drains of the preamplifier. In the test structure of the preamplifier the instability problem has not been encountered. Most probably this is due to the termination in the 50 Ω measurement system instead of the 25 Ω ratrace.

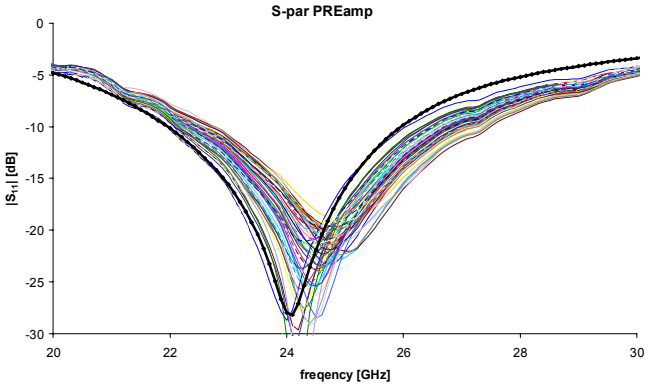

Fig. 5 Input matching of the LO circuit

The measurements of the ratrace test structure show a shift of 3 GHz to higher frequencies (Fig. 3, Fig. 4). This has been observed in more measurements on circuits and test structures. A clear explanation has not been found yet. Especially the

amplitude unbalance at the design frequency will result in less than expected fundamental suppression. This should be better at higher frequencies as has been shown both by resimulation with results of the test structure and measurements of the complete LO chain.

TABLE 1
BIAS SETTING FOR THE LO CHAIN. CURRENT HAS BEEN MEASURED AT THE -1 DB COMPRESSION POINT.

	Vgate [V]	Vdrain [V]	Idrain [mA]	Pdiss [mW]
stage 1	-0.25	3.0	12	36
stage 2	-0.25	3.0	34	102
stage 3	-0.7	3.0	93	279
stage4	-0.25	3.0	47	141
total				558

DC settings as indicated in Table 1 have been determined from the supplied process control monitor (PCM) data of the wafer. These settings have been used for all measurements. Small signal S-parameters and nominal DC currents have been measured on all test cells present on the wafer. The output power and P_{-1dB} at the output have been measured separately with a calibrated power meter.

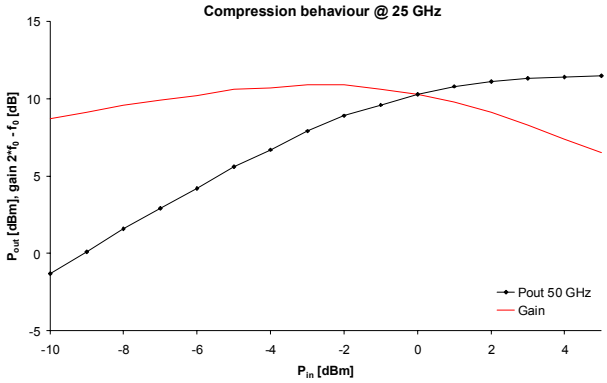

Fig. 6 Measured gain and output power on one sample.

In the final paper output power and fundamental suppression on more samples will be available.

The fundamental suppression is not as initially simulated for 24 GHz; at 25 GHz a better suppression of around 35 to 40 dBc has been measured, depending on the sample (see Table 2 for a good sample).

TABLE 2 MEASURED OUTPUT POWER AND FUNDAMENTAL SUPPRESSION ON TWO SAMPLES AT THE DESIGN FREQUENCY AND AT 25 GHZ

	24 GHz	25 GHz
$P_{-1dB,out}$ [dBm]	8.5 9.5	10.7 11.2
$P_{2f0} - P_{f0}$ [dBc]	31.0 39.9	39.8 42

V. CONCLUSIONS

An LO chain is reported with an excellent fundamental suppression of 35 dB and a gain of 11 dB. The output power at the 1 dB compression point is 11 dBm. The suppression of the fundamental frequency is obtained with a ratrace hybrid at the fundamental frequency. Therefore low losses after the doubler are realised and only one extra amplification stage is enough to drive the mixer.

Measurements showed a shift towards higher frequencies. The reason for this is to be investigated, due to this same reason the best fundamental suppression is obtained at higher frequency than the design frequency.

REFERENCES

[1] ECMA press release, http://www.ecma-international.org/activities/Communications/ga-2007-015.pdf.

[2] G.F. Engen, C.A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyser", IEEE Trans. Microwave Theory and Tech., Vol MTT-27, No. 12, pp. 897-993, December 1979.