X-band Robust AlGaN/GaN Receiver MMICs with over 41 dBm Power Handling

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Abstract— **Gallium-Nitride technology is known for its high power density and power amplifier designs, but is also very well suited to realize robust receiver components. This paper presents the design and measurement of a robust AlGaN/GaN Low Noise Amplifier and Transmit/Receive Switch MMIC. Two versions of both MMICs have been designed in the Alcatel-Thales III-V lab AlGaN/GaN microstrip technology. One chipset version operates at X-band and the second also shows wideband performance. Input power handling of >46 dBm for the switch and >41 dBm for the LNA have been measured.**

I. INTRODUCTION

The wide bandgap semiconductor technology Gallium-Nitride (GaN) is well known for its high power density and many High Power Amplifier designs [1] [2]. Because of the large breakdown voltage of HEMT device realized in the AlGaN/GaN technology, it is also possible to use this technology to design robust receiver components. GaN technology has already shown the capability for low noise performance [3], and even with a technology optimized for high-power applications, good and robust Low Noise Amplifiers (LNA) can be realized [4] [5]. Because of the high power handling also switches can be designed that could replace the current ferrite circulators in Transmit/Receive (TR) modules [6]. This paper will present the design and first iteration measurement results on two LNA and two switch MMICs, which can be used to realize a robust receiver front end. First in section II the application of these MMICs in a TR module front-end is described. Section III gives details on the AlGaN/GaN processing technology. Next the LNA and switch designs are described, followed by the measurement results on these MMICs.

II. ROBUST RECEIVERS

Current TR modules for radar and telecommunication applications usually include a ferrite circulator/isolator, which is a costly and bulky component. This circulator is needed to protect the HPA against unwanted reflections from the antenna and to provide a constant 50 Ω load for the HPA. A GaN HPA, with some form of output protection circuit or dynamic matching would no longer need this circulator, which can then be replaced by a GaN TR switch, see figure 1. On the receive side a limiter is needed to protect the GaAs LNA against too high input power. This limiter is often realized with discrete and expensive components, such as PIN diodes and limits the incoming signal power at 15 – 20 dBm [8]. As will be shown in section VI, GaN LNAs can withstand input power levels up to 41 dBm and a smaller limiter or no limiter at all could be used. Overall this will result in smaller, more light-weight and finally cheaper TR modules.

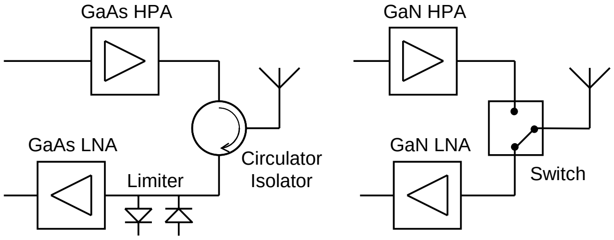

Fig. 1 Example of a classical GaAs front end and robust GaN front end.

III. ALGAN/GAN PROCESSING TECHNOLOGY

The MMICs have been processed on a multi-project wafer in the high-power AlGaN/GaN technology of the Alcatel-Thales III-V lab. The electrical isolation of devices was performed by helium implantation. Ti/Al/Ni/Au ohmic contacts were formed using rapid thermal annealing at temperature of 900°C. Mean contact resistance extracted from TLM measurement is 0.21 Ω.mm. Mo-based T-gates with 0.25 µm length were defined by electron beam lithography. The devices were then passivated using plasma enhanced chemical vapour deposition (PECVD) of SiO_2/Si_3N_4 at a temperature of 340°C. Interconnects were made with evaporated Ti/Pt/Au and electroplated gold for the 3D interconnects (bridges). Passive elements consist in PECVD nitride MIM capacitors, NiCr resistors and evaporated Ti/Pt/Au inductances. After front side processing, the SiC wafer was mounted on a sapphire substrate and thinned down to 100 µm. Plasma etching via-holes technology was used to ground the devices. Vias and back side metallization consisted in sputtered TiW/Au and Au plating.

IV. LNA DESIGNS

Two robust low noise amplifiers have been designed. The first (version 1) is based on 4x50 µm devices and the second version is based on 4x75 µm devices. Both LNAs consist of two stages. The key goals were to design X-band LNAs with 1.2 dB target noise figure and more than 17 dB gain. Power handling is an important specification, which is targeted at 41 dBm input power without damage.

A. LNA version 1

The first LNA version, based on 4x50 µm devices is a straightforward design. A photograph of the LNA is presented in figure 2. The first stage is matched for noise performance by employing source degeneration to bring Γ_{opt} for noise figure matching and S_{11} together. The second stage of this LNA version is designed for maximum gain. Gain flattening is achieved by selective mismatch in the specified frequency band.

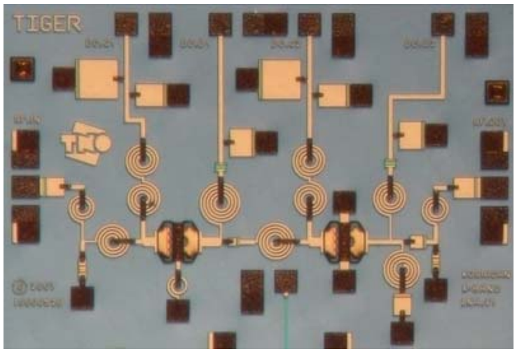

Fig. 2 Microscope photograph of LNA version 1, based on 4x50 µm devices. Die size = 2300 µm x 1500 µm.

B. LNA version 2

The second LNA version based on 4x75 µm devices, shown in figure 3, is also a two stage design. The first stage is again designed for best noise performance by applying a source inductor as source degeneration. The second stage is a feedback stage with an RLC feedback between the drain and the gate. This feedback is used to flatten the gain over a large bandwidth.

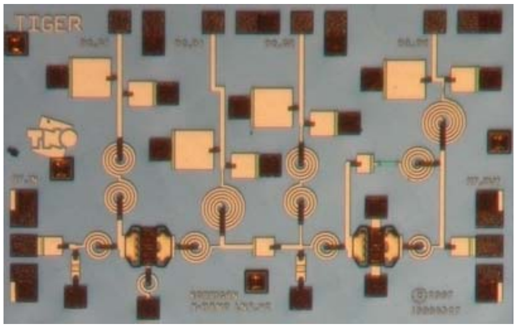

Fig. 3 Microscope photograph of LNA version 2, based on 4x75 µm devices. Die size = 2300 µm x 1500 µm.

V. SPDT SWITCH DESIGNS

Two versions of a single pole double throw (SPDT) switch were designed. Main targets for the switch designs are an insertion loss of 1.0 dB and an isolation of better than 30 dB. The 1 dB compression point specification is targeted on 43 dBm. Momentum based transistor models were used for the design [6].

C. SPDT switch version 1

The topology of version 1 is based on a single series – shunt configuration to keep the insertion loss low. Parallel resonance of the parasitic capacitor of an off-state device with an inductor is employed to improve the isolation of the off-state branch and insertion loss for the on-state branch.

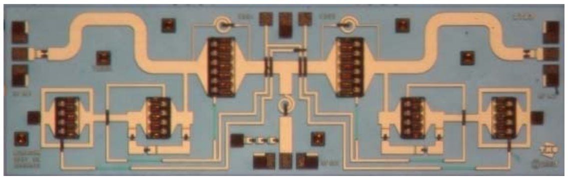

Fig. 4 Microscope photograph of SPDT switch version 1. Die size = 4300 µm x 1300 µm.

D. SPDT switch version 2

The topology of switch version 2 is based on a series – shunt – series configuration to achieve a high isolation. An extra R-C-R branch is applied to add an extra pole for better isolation [7]. One of the shunt devices is capacitor-shunted and the other one is inductor-shunted. This topology provides isolation over a very wide frequency band from DC up to X-band.

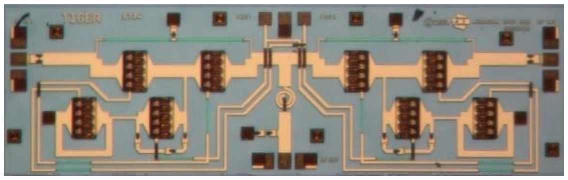

Fig. 5 Microscope photograph of SPDT switch version 2. Die size = 4300 µm x 1300 µm.

VI. MEASUREMENT RESULTS

Small and large signal measurement results of the LNAs and SPDT switches are presented in this section. During the design there were no large signal models available, so there is no comparison with the simulation results for these measurements.

A. Low noise amplifiers

First small signal measurements of both LNAs are presented in figure 6 and 7. Large signal and damage measurements are presented in figure 8 and 9. Both LNAs are biased at Vd = 15 V and Id = 20 mA.

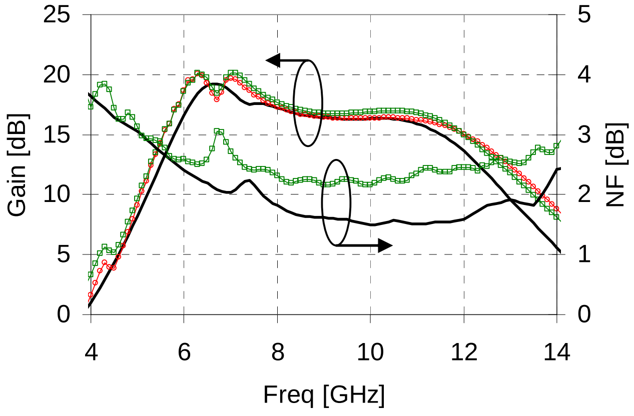

Fig. 6 Gain (left axis) and noise figure (right axis) of LNA version 1. The thick black lines are the simulation results.

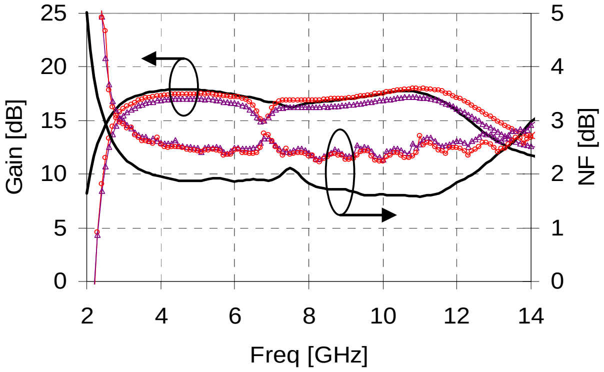

Fig. 7 Gain (left axis) and noise figure (right axis) of LNA version 2. The thick black lines are the simulation results.

The CW large signal measurements show soft compression of the LNAs. The saturated output power is >25 dBm for both amplifiers. Pulsed power damage tests (5 μs pulse width, 10% duty cycle) are carried out with and without a large gate resistance of 8.2 kΩ in the first stage [4]. Figure 9 shows a significant robustness improvement when a large gate resistance is applied to reduce forward gate current.

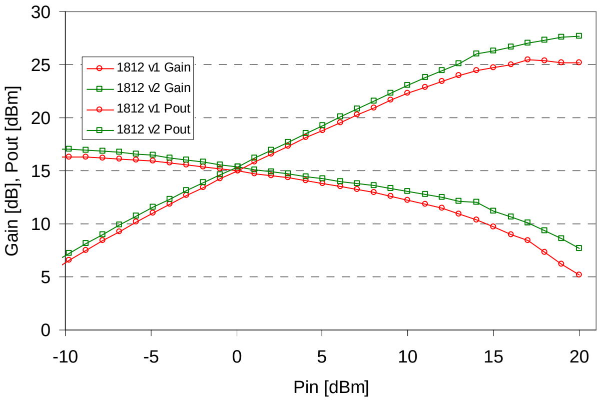

Fig. 8 CW input power versus output power and gain of both LNA versions.

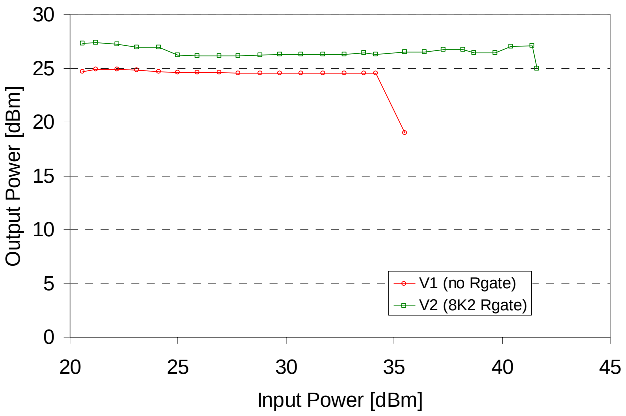

Fig. 9 Pulsed power measurement results of the damage test of both LNAs.

The small signal measurement results of both SPDT switches are presented in figure 10 to 13. The large signal measurement results are shown in figure 14 and 15. The off-state voltage of the switch devices is -20 V and for on-state the gate is set to 0 V.

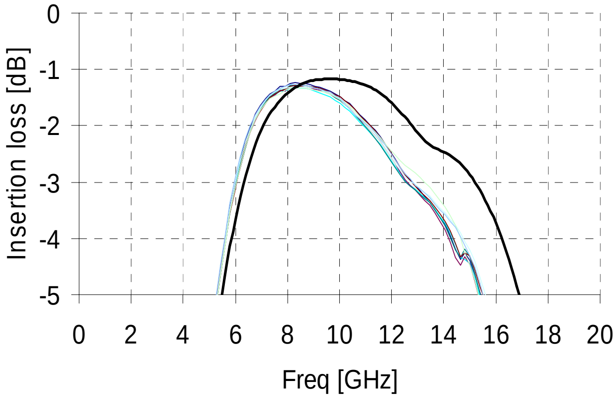

Fig. 10 Insertion loss measurement results of SPDT switch version 1. Thick black line is the simulation.

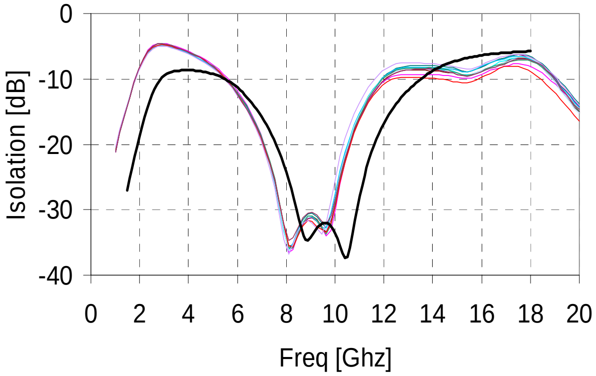

Fig. 11 Isolation measurement results of SPDT switch version 1. Thick black line is the simulation.

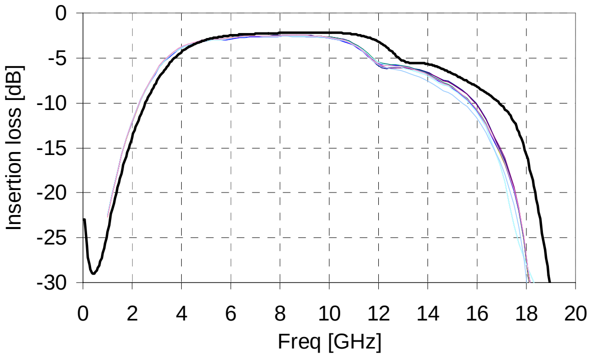

Fig. 12 Insertion loss measurement results of SPDT switch version 2. Thick black line is the simulation.

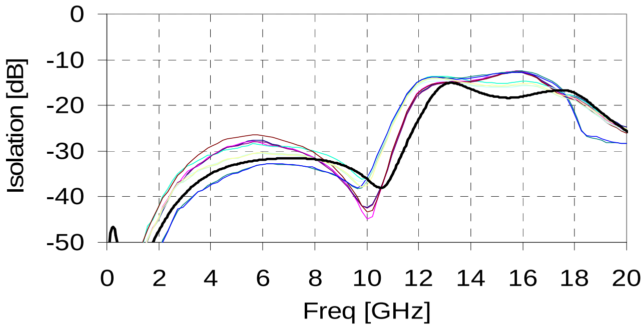

Fig. 13 Isolation measurement results of SPDT switch version 2. Thick black line is the simulation.

Pulsed large signal measurements show a 1 dB compression point of 43 dBm for version 1 and 40 dBm for version 2 with different duty cycles. The pulse width has been swept from 5 µs (5 % duty cycle) to 30 µs (30 % duty cycle). Our power measurement setup (max 46 dBm) is not able to damage the switches.

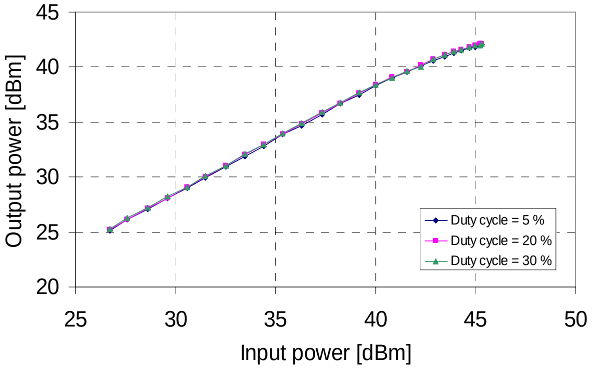

Fig. 14 Power sweep measurement results of SPDT switch version 1 with different duty cycles.

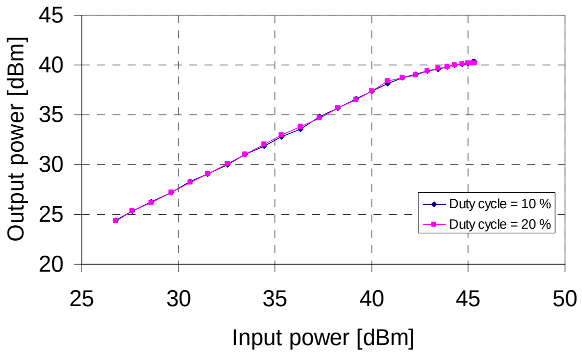

Fig. 15 Power sweep measurement results of SPDT switch version 2 with different duty cycles.

VII. CONCLUSIONS

Robust LNAs and SPDT switches are successfully designed in GaN microstrip technology. The measurement results of the first design iteration show a good match with the simulation results. Both low noise amplifiers show a noise figure of 2.3 dB in X-band and have more than 16 dB gain. The LNAs are able to survive more than 10 W input power. The SPDT switches are able to handle an input power of more than 46 dBm without any damage. These results show that GaN technology enables realisation of robust receiver components.

ACKNOWLEDGMENT

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