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(54) A phased array antenna signal processing structure, a method and a computer program product

(57) The invention relates to a phased array antenna signal processing structure. The structure comprises a processor that includes a digital beam forming unit for generating partial beam data from digitized samples of a set of phased array antenna elements. The processor further comprises a set of input terminals for receiving intermediate beam data from another processor. The processor also comprises an adder for generating new intermediate beam data by adding partial beam data generated by the digital beam forming unit to corresponding received partial beam data. In addition, the processor comprises a set of output terminals for transmitting the new intermediate beam data.

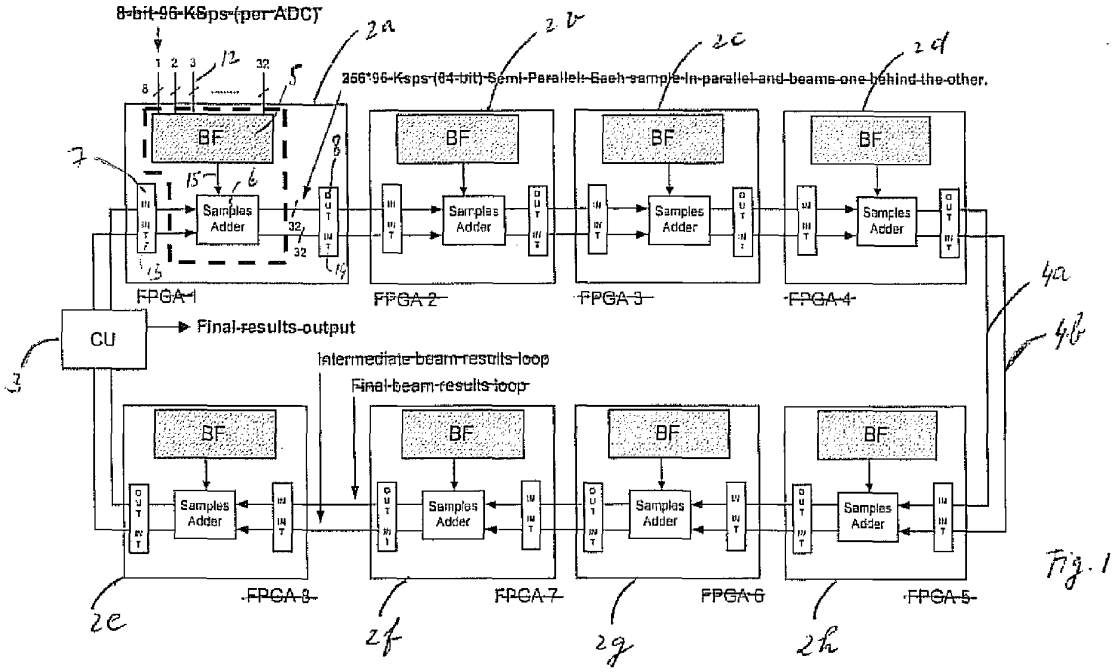

Fig. 1

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Description

[0001] The invention relates to a phased array antenna signal processing structure, comprising a processor that includes a digital beam forming unit for generating partial beam data from digitized samples of a set of phased array antenna elements.

[0002] Digital beam forming in active electronic antenna arrays is complex. When the beam forming is performed in the digital domain, a central processor is heavily loaded both in terms of processing load and in communication load. Current implementations of analog and digital beam formers are very inflexible and poorly scalable. When the number of (phased array) antenna elements increases, the computational requirements of the used processor increases exceptionally.

[0003] It is an object of the invention to provide a more efficient signal processing structure according to the preamble for processing phased array antenna element data. Thereto, according to the invention, the processor further comprises a first set of input terminals for receiving intermediate beam data from another processor, a first adder for generating new intermediate beam data by adding partial beam data generated by the digital beam forming unit to corresponding received intermediate beam data, and a first set of output terminals for transmitting the new intermediate beam data.

[0004] By both generating partial beam data and adding intermediate beam data from another processor, the processing capacity as well as the communication load of the signal processing structure can be distributed, thereby optimally exploiting the processor capacity. Especially when the processors are communicatively connected in a ring structure for cyclically performing the adding function, all processors can in principle be loaded equally.

[0005] The processing functions that are needed for computing a digital beam can be effectively distributed over the available processors. Further, the processor according to the invention allows a highly scalable ring structure wherein the number of processors increases linearly with number of phased array antenna elements and the communication load remains the same. The structure is thus fully scalable regarding the number of digital beams, the number of phased array antenna elements and the number of processors. In addition, since only intermediate results are transmitted, there is a low communication load on array level while the communication between the processors is minimal. Further, a hierarchical beam forming structure can be realized without a hierarchy in the processor structure.

[0006] Further, the invention relates to a method for processing.

[0007] In addition, the invention relates to a computer program product. A computer program product may comprise a set of computer executable instructions stored on a data carrier, such as a flash memory, a CD or a DVD. The set of computer executable instructions, which allow a programmable computer to carry out the method as defined above, may also be available for downloading from a remote server, for example via the Internet.

[0008] Other advantageous embodiments according to the invention are described in the following claims.

[0009] By way of example only, embodiments of the present invention will now be described with reference to the accompanying figures in which

Fig. 1 shows a schematic view of a phased array antenna signal processing structure according to the invention;
Fig. 2 shows a schematic view of a compressor in the structure of Fig. 1;
Fig. 3 shows a schematic view of three subsequent processors in the structure of Fig. 1; and
Fig. 4 shows a flow chart of a method according to the invention.

[0010] The figures are merely schematic views of a preferred embodiment according to the invention. In the figures, the same reference numbers refer to equal or corresponding parts.

[0011] Figure 1 shows a schematic view of a phased array antenna signal processing structure 1 according to the invention. The structure 1 includes a multiple number of identical processors 2a-h that are communicatively connected in a ring structure. In the shown embodiment, the ring structure is composed of eight processors 2a-h and a central unit that are interconnected via two sets of communication lines 4, viz. a set of communication lines 4a transmitting intermediate beam data and a set of communication lines 4b transmitting final beam data. The set of communication lines 4a,b can be physically distinct lines or logically distinct lines.

[0012] Figure 2 shows a schematic view of a processor 2 from the ring structure 1. The processor 2, also called tile, includes a digital beam forming unit 5, also called beamformer, for generating partial beam data from digitized samples of a set of phased array antenna elements. Further, the processor 2 includes a first adder 6, also called samples adder, for adding the generated partial beam data. In addition, the processor 2 includes a number of terminals for communication with other devices.

[0013] More specifically, the processor 2 includes a first set of input terminals 7 for receiving intermediate beam data 44a from a preceding processor in the ring 1, a first set of output terminals 8 for transmitting new intermediate beam data 44a to a subsequent processor in the ring 1, a second set of input terminals 9 for receiving digitized samples 12 of a phased array antenna set, a third set of input terminals 10 for receiving digital beam coefficients 11, a fourth set of input terminals 13 and a second set of output terminals 14 for receiving and transmitting, respectively, final beam data 44b.

[0014] In order to obtain the ring structure, the first set of input terminals 7 of a particular processor 2c are con-

nected the first set of output terminals 8 of a preceding processor 2b in the ring 1. Similarly, the first set of output terminals 8 of the particular processor 2c are connected to the set of input terminals 7 of a subsequent processor 2d in the ring 1. Analogously, the fourth set of input terminals 13 and the second set of output terminals 14 of subsequent processors 2 in the ring structure 1 form the second set of communication lines for the final beam data 44b.

[0015] Each processor 2 contains the same number of input terminals in the second set of input terminals 9, so that each processor can process the same number of samples 12. In the shown example, the processor 2 includes 32 first input terminals 9, also called sample input channels. Then, the ring structure 1, including in the shown example 9 processors 2, is able to process 256 channels of digital samples. Thereto, a phased array antenna structure is split into 8 sets of phased array antenna elements, each feeding a corresponding processor 2.

[0016] Also the central unit 3 is provided with corresponding sets of input terminals and output terminals for receiving the intermediate beam data 4a and the final beam data 4b.

[0017] During operation of the ring structure 1 according to the invention, each processor 2a-h receives, via the second set of input terminals 11 digitized samples 12 from the corresponding set of phased array antenna elements. Thereto, the samples have been digitized using analog to digital converters ADC's. Each processor 2 processes the samples 12 to generate partial beam data. In this process, digital beam coefficients 11 are received via the third set of input terminals 10. The digital beam forming unit 5 includes a set of multipliers for multiplying the received samples 12 with corresponding digital beam coefficients 11. Further, the digital beam forming unit 5 includes a second adder for adding corresponding multiplied samples to generate partial beam data.

[0018] In order to obtain a digital beam, each sample is multiplied with a corresponding coefficient. Then, all multiplied samples are added. Thus, in each processor 2 receiving, in the shown embodiment, 32 samples, 32 multiplied samples are added. However, according to an aspect of the invention, a multiple number of digital beams can be computed. Thereto, the same samples 12 are also multiplied with other digital beam coefficients 11 to arrive at a second set of digital beam data. Preferably, the number of digital beams is in the same order as the total number of samples, in this example, 256 digital beams. The data that is generated in the digital beam forming unit 5 are called partial beam data, since the adding process has not yet been performed over all samples, but only over the samples that are received by a common processor 2. In the following, the process of adding the partial beam data is described.

[0019] The partial beam data 15 is internally transmitted to the first adder 6 that receives also intermediate beam data 44a from the preceding processor 2 in the ring structure 1, via the first set of input terminals 9. Using the first adder, the partial beam data 15 generated by the digital beam forming unit 5 is added to the intermediate beam data 44a to get a new update of the intermediate beam data 44a. Corresponding digital beam data are added, i.e. a summation is performed over partial beam data that relate to the same digital beam. The new update of the intermediate beam data 44a is transmitted to the next processor 2 in the ring structure 1. When this process is repeated, subsequently, by the eight processors 2, all digital beams have been computed. The data of the complete digital beams are called final beam data 44b.

[0020] According to an aspect of the invention, final beam data are generated by adding intermediate beam data received at a processor to corresponding partial beam data generated by the processor, wherein the intermediate beam data are based on corresponding partial beam data generated by all other processors in the ring 1. The final beam data 44b is transmitted via the second set of output terminals.

[0021] Figure 3 shows a schematic view of three subsequent processors 2a-c in the structure 1. According to an advantageous embodiment of the invention, the computation of the final beam data 44b is evenly distributed over the processors 2, so that each processor 2 performs a similar task. In the exemplary embodiment, each processor 2 generates 32 different final digital beams adding up to the total number of 256 digital beams. In the shown embodiment, the first processor 2a computes a block 80 of final digital beams, viz. digital beams 225-256, and seven blocks 81 of 32 intermediate digital beam data each. Similarly, the second processor 2 b computes a single block 80 of other final digital beams, viz. digital beams 193-224, and seven blocks 81 of 32 intermediate digital beam data each. The block 80 that is added, by a particular processor 2, to the communication line 4b of final data, is not changed by the other processors 2.

[0022] The central unit 3 obtains all blocks of final data 44b for further processing. The fully beam formed data referred to as final beam data available for further processing can be transmitted to units outside the ring structure. In a first embodiment, the final beam data can be transmitted to a single processor unit. However, the communication load is herewith locally increased. In a further embodiment, the final beam data are transmitted to a dedicated processor node embedded at any location in the ring structure. In yet a further embodiment, one or a few beam data sets are allocated to a single processor, so that the communication load is distributed over available processors. The latter method of communicating final beam data has the added advantage that any additional processing required per final beam data set (e.g. range-doppler processing) can be equally divided over processors as well. In order to facilitate a proper time management of the data to be processed and transmitted, a number of further input terminals and output terminals can be provided. As an example, the processor might include terminals for time controlling signals and/or for reading data such as multiplication coefficients that

have been input to the processor.

[0023] It is noted that, preferably, the number of first and second input terminals, and the number of first and second output terminals coincides to optimally benefit from digital I/O terminals in the processor 2. In a different embodiment the data passed between processors can contain time stamp data to align partial beam data and intermediate beam data.

[0024] As an example, the digital samples are received at a rate of 96 K samples per second, per ADC, each sample having 8 bits that are transmitted serially.

[0025] According to a further aspect of the invention, a defect in the performance of a specific processor in the ring structure can be detected. Then, the intermediate data and the final data can be transmitted by a preceding processor in the ring, towards a subsequent processor in the ring, thus circumventing the processor having the defect. Apparently, measures have to be taken to properly delay the data or time stamp the data, so that the other processors continue in meaningfully processing the intermediate results. Advantageously, by applying a data transfer by-pass, the ring structure can continue processing phased array antenna data, also with a defect processor, albeit with a reduced performance since the functionally eliminated processor and connected antenna element data do not contribute anymore in computing a digital beam.

[0026] In this respect it is noted that the steps of detecting a defect in the performance of a specific processor, and forwarding the intermediate data and final data transmitted by a preceding processor towards a subsequent processor can not only be performed in combination with a phased array antenna signal processing structure wherein a multiple number of processors are communicatively connected in a ring structure, but also, in combination with a more general phased array antenna signal processing structure wherein a multiple number of processors are communicatively connected in a chain structure.

[0027] The processor can be implemented in various ways, e.g. as an FPGA, an ASIC, a DSP or a general purpose processor, e.g. using a laptop.

[0028] Figure 4 shows a flow chart of an embodiment of the method according to the invention. The method is used for processing phased array antenna digitized samples. The method comprises the steps of generating (100) partial beam data using a processor processing a digitized samples received from a set of phased arrays, receiving (110), at the processor, intermediate beam data from another processor processing digitized samples received from another set of phased array antenna elements, generating (120) new intermediate beam data by adding the partial beam data to the corresponding received intermediate beam data, and transmitting (130) the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased arrays.

[0029] The method of processing phased array antenna digitized samples can be performed using dedicated hardware structures, such as FPGA and/or ASIC components. Otherwise, the method can also at least partially be performed using a computer program product comprising instructions for causing a processor of the computer system to perform the above described steps of the method according to the invention. All steps can in principle be performed on a single processor. However it is noted that at least one step can be performed on a separate processor, e.g. the step of transmitting the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased arrays.

[0030] The invention is not restricted to the embodiments described herein. It will be understood that many variants are possible.

[0031] It is noted that another number of processors and another total number of samples can be chosen. Further, another number of input terminals in the second set of input terminals of the processors can be chosen.

[0032] In addition, the processor can include further processing functions such as analog-digital conversion, calibration etc. Calibration can be implemented as an additional multiplication, for the sake of a simple design, or as an additional addition, for the sake of computational efficiency.

[0033] The digital beam forming unit can process on the real and imaginary part of the samples. Otherwise, also the amplitude and phase components can be processed. Further, by signal decomposition in frequency and phase components, an efficient Hilbert operation can optionally be applied.

[0034] Other such variants will be apparent for the person skilled in the art and are considered to lie within the scope of the invention as determined in the following claims.

Claims

1. A phased array antenna signal processing structure, comprising a processor that includes a digital beam forming unit for generating partial beam data from digitized samples of a set of phased array antenna elements, and wherein the processor further comprises:

    - a first set of input terminals for receiving intermediate beam data from another processor;
    - a first adder for generating new intermediate beam data by adding partial beam data generated by the digital beam forming unit to the corresponding received intermediate beam data ;
    - a first set of output terminals for transmitting the new intermediate beam data.

2. A structure according to claim 1, wherein the processor comprises:

- a second set of input terminals for receiving the digitized samples of a phased array antenna set;
- a third set of input terminals for receiving digital beam coefficients; and wherein the digital beam forming unit comprises a set of multipliers for multiplying the received samples with corresponding digital beam coefficients; and
- a second adder for adding corresponding multiplied samples to generate partial beam data.

3. A structure according to claim 1 or 2, wherein the partial beam data and the intermediate beam data include data relating to multiple digital beams.

4. A structure according to any of the preceding claims, comprising a multiple number of processors communicatively connected in a ring structure.

5. A structure according to claim 4, wherein the first set of input terminals of a particular processor are connected to the first set of output terminals of a preceding processor in the ring, and wherein the first set of output terminals of the particular processor are connected to the first set of input terminals of a subsequent processor in the ring.

6. A structure according to claim 4 or 5, wherein each of the processors are arranged for processing samples of a corresponding set of phased array antennas.

7. A structure according to any of claims 4-6, wherein each processor contains the same number of input terminals in the second set of input terminals.

8. A structure according to any of claims 4-7, further comprising a central unit, included in the ring, for receiving final beam data.

9. A structure according to any of claims 4-8, wherein the processors further include a fourth set of input terminals and a second set of output terminals for receiving and transmitting, respectively, final beam data.

10. A structure according to any of claims 4-9, wherein the adder in each processor is arranged for generating final beam data by adding received intermediate beam data to corresponding partial beam data generated by the digital beam forming unit wherein the intermediate beam data is based on corresponding partial beam data generated by all other processors in the ring.

11. A structure according to any of claims 4-10, wherein the processors are identical.

12. A method for processing phased array antenna digitized samples, comprising the steps of:

- generating partial beam data using a processor processing a digitized samples received from a set of phased array antenna elements;
- receiving, at the processor, intermediate beam data from another processor processing digitized samples received from another set of phased arrays;
- generating new intermediate beam data by adding the partial beam data to the corresponding received intermediate beam data; and
- transmitting the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased arrays.

13. A method according to claim 12, further comprising the steps of:

- splitting the digitized samples of the phased array antennas into a multiple number of N digitized sample sets;
- generating partial beam data using N processors communicatively connected in a ring structure, each processor processing a corresponding digitized sample set;
- receiving, at each processor, intermediate beam data from a preceding processor in the ring;
- generating, by each processor, new intermediate beam data by adding the intermediate beam data that is received at each processor to corresponding partial beam data generated by said processor; and
- transmitting all new intermediate beam data to the subsequent processor in the ring.

14. A method according to claim 13, further comprising generating final beam data by performing the steps of:

- adding intermediate beam data received at a processor to corresponding partial beam data generated by the processor wherein the intermediate beam data are based on corresponding partial beam data generated by all other processors in the ring; and
- deciding whether the added intermediate beam data is complete and can be transferred as final beam data instead of intermediate beam data.

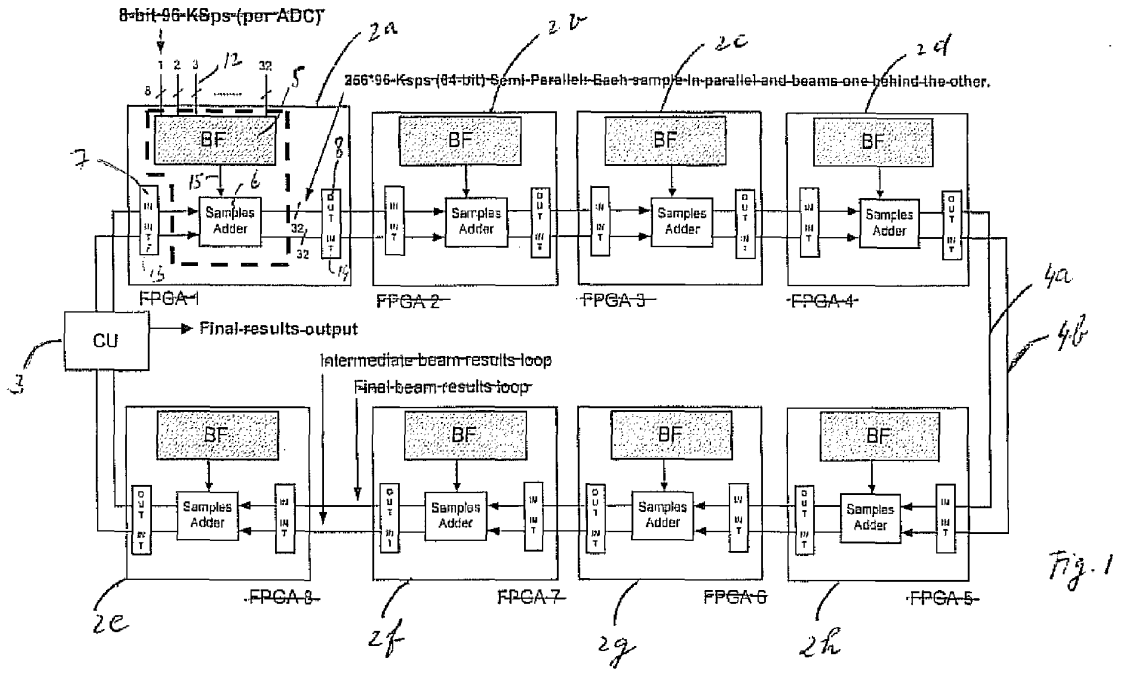
15. A method according to claim 14 , further comprising a step of performing additional processing on the final beam data.

16. A method according to claim 15, further comprising

detecting a defect in the performance of a specific processor in the ring structure, and forwarding the intermediate data and final data transmitted by a preceding processor in the ring, to a subsequent processor in the ring.

17. A computer program product for processing phased array antenna digitized samples, the computer program product comprising computer readable code for causing a processor to perform the steps of:

- generating partial beam data using a processor processing a digitized samples received from a set of phased array antenna elements;
- receiving, at the processor, intermediate beam data from another processor processing digitized samples received from another set of phased arrays;
- generating new intermediate beam data by adding the partial beam data to the corresponding received intermediate beam data; and
- transmitting the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased array antenna elements.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BF
Samples Adder
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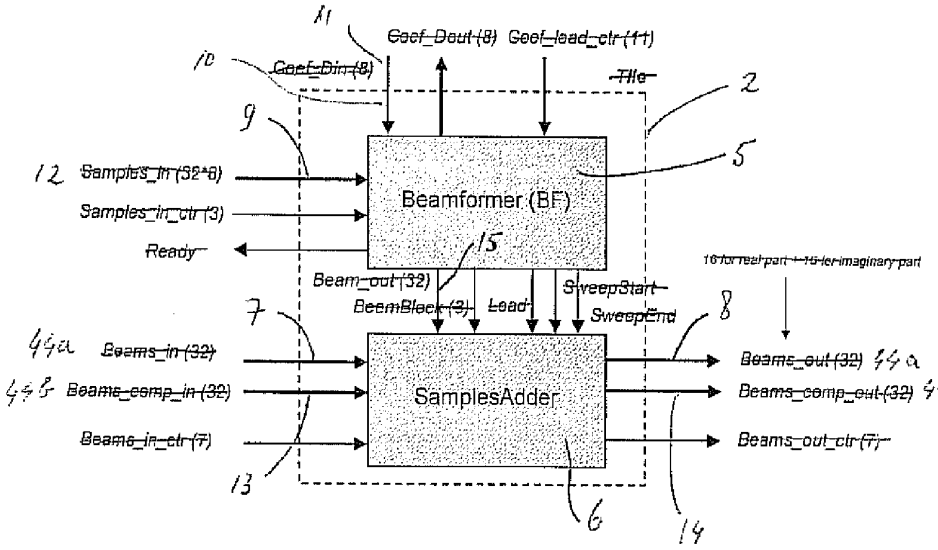
FPGA-2
FPGA-3
FPGA-4
FPGA-5
FPGA-6
FPGA-7
FPGA-8
CU
Final-results-output
Intermediate-beam-results-loop
Final-beam-results-loop

Fig. 1


11
Coef_Dout (8)
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File
2
9
5
12
Samples_in (32*8)
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Ready
Beamformer (BF)
15
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Beam_out (32)
BeamBlock (3)
Load
SweepStart
SweepEnd
7
8
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Beams_in (32)
49b
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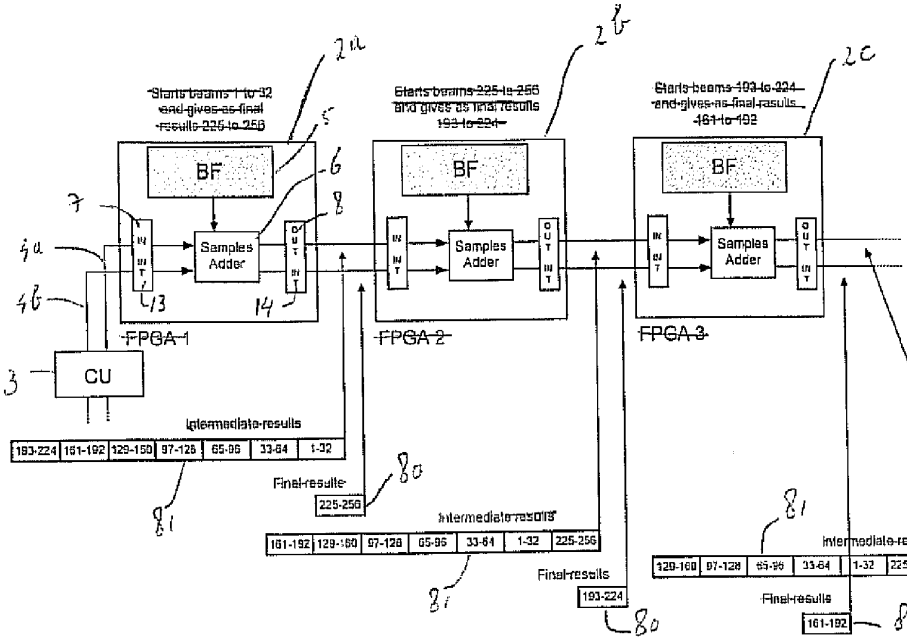
6
14

Fig. 2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Starts beams 225 to 256 and gives as final results 193 to 224
Starts beams 193 to 224 and gives as final results 161 to 192
BF
Samples Adder
FPGA 1
FPGA 2
FPGA 3
CU
Intermediate results
193-224 161-192 129-160 97-128 65-96 33-64 1-32
Final results
225-256
161-192 129-160 97-128 65-96 33-64 1-32 225-256
193-224
129-160 97-128 65-96 33-64 1-32 225-256 193-224
161-192

Fig.3

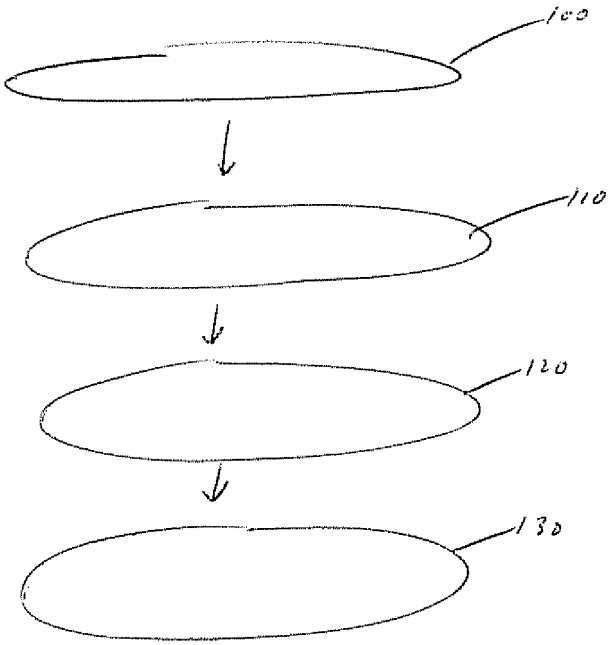

Fig. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 10 15 7564

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	WO 2004/030145 A1 (ERICSSON TELEFON AB L M [SE]; FALK KENT [SE]; KARLSSON INGMAR [SE]; LI) 8 April 2004 (2004-04-08) * abstract * * page 1, line 7 - page 7, line 27 * * page 12, line 19 - page 13, line 31; figures 3A,3B * * page 19, paragraph 2; figure 8 * -----	1-17	INV. H01Q21/00
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TECHNICAL FIELDS SEARCHED (IPC)

H01Q

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	24 August 2010	Yang, Betty

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24-08-2010

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