LTCC Phase shifter modules for RF-MEMS-switch integration

Thomas Bartnitzek*, Edda Müller *, Raymond van Dijk **
*VIA electronic GmbH, Hermsdorf, Germany **TNO Defence Security and Safety, The Hague, NL
Robert- Friese- Straße 3, D-07629 Hermsdorf
Tel.: +49 36601 81529, Fax: +49 36601 81530, Email: t.bartnitzek@via-electronic.de

Abstract

The European IST project ARHMS is covering a wide field of R&D activities with the final goal: a satellite based car communication system with a flat electronically steerable roof antenna based on RF-MEMS. The required phase shift for beam steering will be done with MEMS switches and RF networks. An integratable LTCC packaging and wiring module with the MEMS and the passives has to be placed and connected close to the patch antenna.

LTCC as a ceramic interconnection technology for processing multilayer boards, multi-chip-modules and packages, enables increased circuit density and high reliable structures. Within this work the good integration opportunities and the low loss of LTCC were reasons for the choice as well as thermal conductivity and the possibility to build cavities and windows, to integrate the RF-switches and SMDs and to guide the RF signal in a power range around 5 watt (Tx).

Initial material studies and investigation, simulations of the RF conditions, technology improvements in structuring and processing LTCC as well as numerous test runs and measurements had been done to develop an initial test substrate. These early test structures were used to verify the design and simulation surrounding. The extracted correlation data allow the most promising layout work.

Key words: packages, MEMS switches, RF networks, LTCC, passives integration

Introduction

Multilayer ceramic materials are well known and frequently used for applications where packaging, wiring and heat dissipation aspects or passives integration, RF behaviour and high integration is requested. In the LTCC substrate described in this paper the combination of all these demands is the real challenge.

The most inviting topic was to find out how it would be possible to integrate the capacitive and inductive structures for the R-L-C networks of several 3-bit-shifters on a small module with minimal size and integrated MEMS switch chips. Their dice should be placed in cavities to wire them wave-guide-friendly on top and with good heat distribution opportunities on bottom.

The development work of the phase shifter module has been shared between VIA electronic as an established LTCC developer and manufacturer and TNO as an institute with knowledge and experience in RF design. It has been structured into the following tasks:

- materials enquiry and selection
- design of test structures , including 50 Ω lines, TRL calibration, inductors, mounting pads for SMD components, sub-circuits (high-pass, low-pass networks) etc. The test structures should reveal all information necessary for the design of the phase shifter demonstrators.
- preparation of a couple of tiles with the complete structure (DuPont / ESL) in different versions
- RF measurements in TNO
- comparison with calculated and designed values and RF performance

Design and Layout

The phase shifter module has to contain RF lines for connection of the components, the passives for the network, the control interface connection as well as the switches. Because 3-bit shifters were needed, with a phase shift of 45°, 90° and 180°, there was a demand for higher capacitance then available with printed structures at 951AT (fired thickness 90µm), which is one of the most common and best controlled tapes in LTCC manufacturing.

The miniaturization request and the parasitic capacitive and inductive behaviour of structures in a package with different GND- and voltage-layers and shieldings brought additional challenges into the development activities. The substrate thickness had to be chosen, because the line width for a 50 Ω microstrip line needed to be calculated; this has to comply with the rule for minimum line width. Tx Line has been used to calculate these parameters.

With one layer the possibility of crossing lines is absent. Four or five layers result in very wide lines, which will hamper small designs and the number of stacked vias for ground connection will exceed the maximum. Therefore the designs has been made for two and three layers of tape.

In the design of matching networks the use of lines with non-50 Ω impedance is used. In hybrids often lines with impedances of √2 and 1/√2 times the characteristic impedance are used. For each different width two lines will be included, with different length. This enables the extraction of line impedance and propagation constant [1]. The length of the lines should be such that both lines can be approximated by a lumped π-circuit at the lowest frequency. In all cases the effective dielectric constant is smaller than 6, and therefore the wavelength,

$$\lambda = \frac{c}{\sqrt{\varepsilon_{eff}}\, f},$$

at 200 MHz, the lower measurement range, is larger than 600 mm. As a rule of thumb structures of 1/20 of the wavelength are considered lumped, and thus all lines shorter than 5 mm will be suited for this purpose. The lengths are chosen to be 2000 µm and 3000 µm.

For the RF networks inductors and capacitors had to be implemented regarding the design rules [2]; the following schematics show possible constructions of the modules.

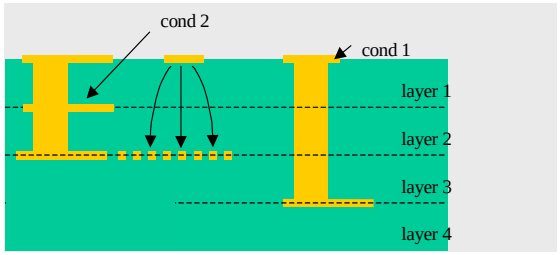

Fig.1: "traditional" structures built up with 951 AT layers with capacitive, inductive, resistive and wave guide structures, i.e. layer thickness with typical k=7.8 of this LTCC

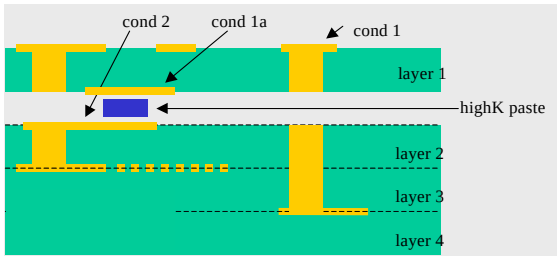

Fig.2: principle of the first type test substrate, containing different test layouts for high-k-paste between 951 AT layers

Test structures and substrates manufacturing

The test structures, based on two layouts with 3 sub-types has been processed with both material systems: the ESL41…and the DuPont 951. Each tape material was used to build up substrates made of gold and ones of silver metallization systems. The layout contains each different sizes, arrangements and versions of capacitors, inductors and resistors with the aim to get information regarding repeatability, tolerances, size-value-ratio and possible limitations. Additionally there are SMD mounting pads, coupled and crossing lines, low and high pass sections and calibration features.

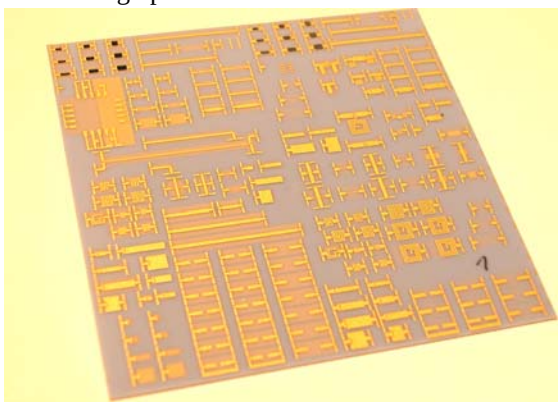

Fig. 3: Overview test structure type 2109, substrate nr. 1

To get an appreciation of this trial run the figures 1 and 2 as well as 6 and 9 later on are illustrating the principle of the different setups. In these cross section drawings it has not been considered the various types of capacitors, which were realized. Different types means that sizes and geometries of plates have been varied, different ratio between upper and lower plate as well as multiple stacks of plate and dielectric have been used.

The first couple of parts following the test design with internal index #2109 has been processed on 18 test substrates. In the ESL system the low loss and low k (k=4.2) tape 41110 has been chosen due to these characteristics as well as the 41020 with standard characteristics [3], [4]. The shrinkage behaviour of the capacitance pastes (ESL 4163 and 4164 have been used with k=100 and 250) in the first trials has not been in a range, where a successful manufacturing of such a complex module seems to be achievable. Known influences to this behaviour have been checked regarding their influence to the result. There were variations in the firing profile (heating gradients, atmosphere, thermal propagation, lamination processes etc.).

As an example for the strong demand for optimization of the capacitive structures a laserscan illustrating the waviness during the first batch can be seen in fig. 4.

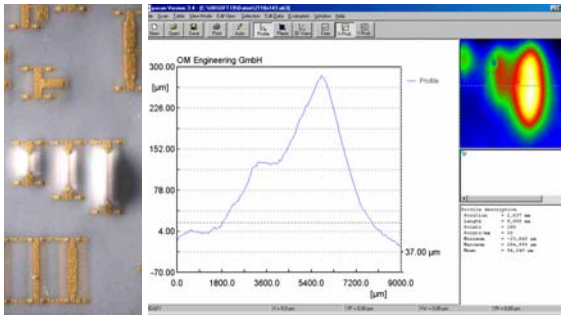

Fig. 4: Photo and laser scan of a sample with strong warping due to extremely thick and asymmetrical integration of 4163 dielectric paste

The scanned surface represents the height difference between local coverage and LTCC without additional paste as well as any overlapped warping. The maximum values of these surface scans lead to a quantitive proposition of the different influences (see fig. 5 and 6). The construction has been varied as well as :

- number of layers
- paste thickness
- structure size

using asymmetric stacks, fig. 5 and a symmetric ones (as required by suppliers) represented in fig.6. In the cross-section like outlines the locally dark parts represent the presence of paste between the lighter layers of LTCC.

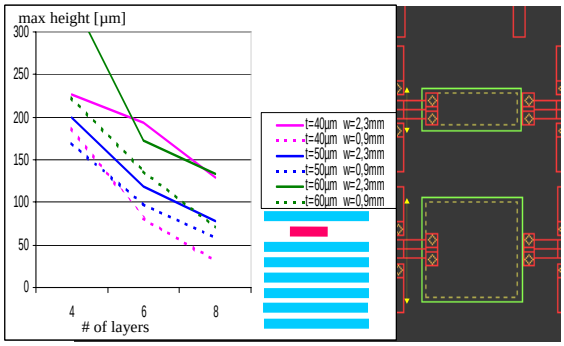

Fig. 5: measurements of maximal height values (reflecting the extend of deformation) over number of layers, while capacitor size and thickness were parameters

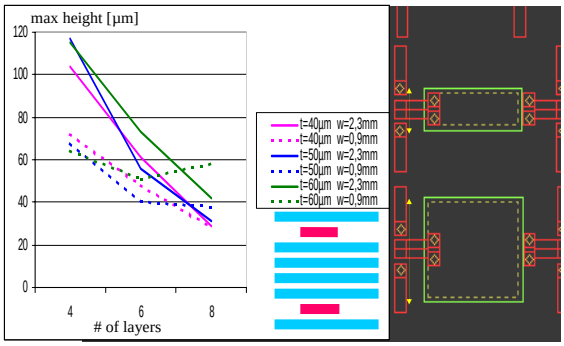

Fig. 6: same measurement at symmetric samples (description cf. fig.5)

After processing the run with high-k paste the problems with the shrinkage behaviour has been interpreted and used for a couple of design rules for this process.

In addition a test run has been made with the high-k tape. To reduce cost the same mask set has been used. Impedances have of course not been 50 Ω, but it still yielded useful tests. The second set of design runs #2118.. has been created for the integration of tape layers which increase the capacitive values.

The ESL high-k tape 41210 has dielectric constant around 100 and a thickness after firing of 100 µm. It has been placed between the top and second layer. The use of vias is possible as well as via filling, although this last step will cause a larger distance between the *original* layers 1 and 2. The tape can be punched away in areas where the origin structure should remain (fig. 7 and 8).

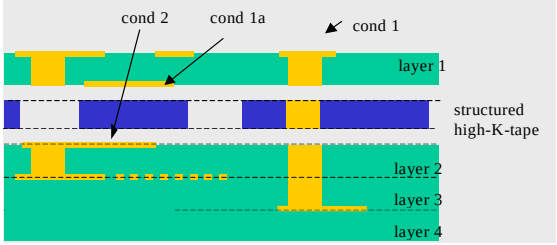

Fig. 7: high-k area created by high-k-tape, punched for local contact of 1st and 2nd layer, where the presence of high-k is not advisable

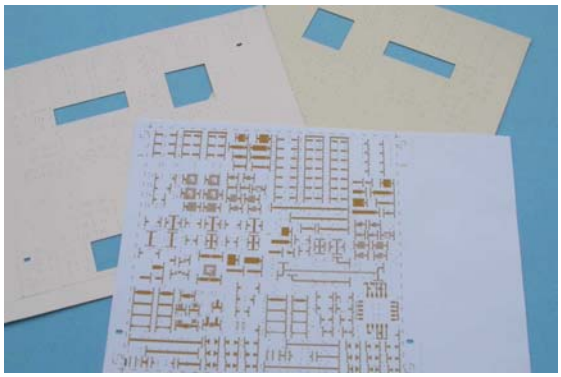

Fig. 8: Au printed top layer 41020 and two different punched dielectric layers made of 41210 and 41250

While the construction with the cut-outs has only been working restricted with one 412.. layer, an additional trial with symmetrical tape as the (n-1)st was – as understandable – more successful. (see fig. 9)

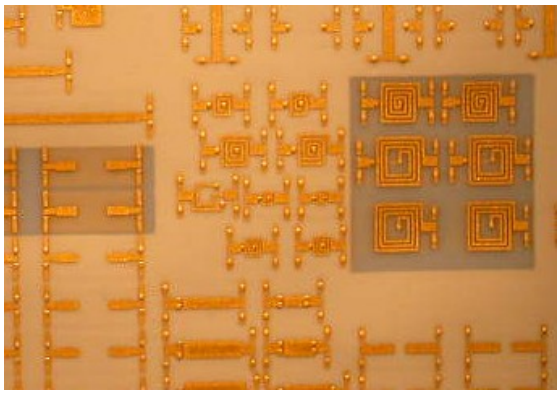

Fig. 9: cutouts in the 41210 tape, visible through the translucide top layer (nr. 26: ESL 41020, 2 x ESL 41210, Au)

An additional opportunity, which has been tested is the use of a very thin LTCC foil of DuPont951, with a fired thickness of about 40µm. The handling of these foils is quit different to "normal" LTCC tape, although it is out of the same material family. Because of its low thickness it is necessary to handle and to process it with its backing, a plastic foil, where the ceramic slurry had been casted on.

All process steps before and including the lamination process need to be adapted to the circumstance, that this plastic is still on the back. This is no problem during punching the holes, but the viafilling fills not only the hole in the tape, but the Mylar® foil too. The Mylar removal is a quite critical process step, because the filling needs to tear off just below the foil on the tape surface. For silver systems there is a special viafilling paste on the market, but not for the gold system[5].

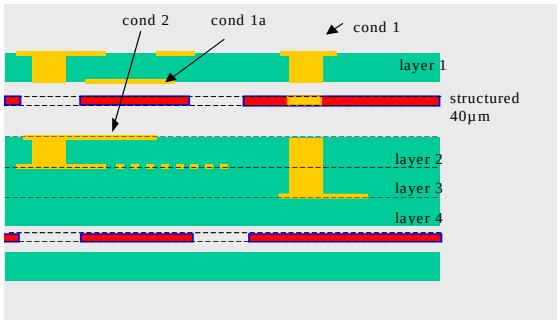

Fig. 10: principle of the stack containing thin 951C2 as the capacitive layer, the (n-1)st seems to be unnecessary after the tests

pros: solid, homogeneous material, the compatibility of the paste materials and the well known shrinkage behaviour.

cons: dielectric constant is the same 7.8 , so only the smaller distance is acting

With the DuPont thin layer series capacitors with a value of 6.5 pF were measured. No excessive loss was seen. The thin layer has little effect on other structures and can be easily used in simulators as the only parameter that changes is the total layer stack; the dielectric constant of the thin layer is identical to the other layers.

Following the request for narrow coils to keep capacitances lower, the layout based on a couple of design features going closer to the limits of the conventional screen printing process. Advanced screens with special emulsion and meshes have been used to achieve acceptable results and yield.

One of the goals was to compare structures, which have been calculated by the simulation tool, with the measurements of real LTCC structures. This procedure has to show some kind of correlation between calculation and the real part as well as a set of new input data for the

simulation program. The mid-term objective is a software-based tool. It shall be able to calculate the best matching parameter set which prevents numerous additional tests.

Measurements

Several different microstrip lines are present in the lay-out. When microstrips are identical in cross section and pad lay-out, but have different lengths, the method described in [1] and [6] can be used to extract the characteristic impedance and transmission line coefficients.

All RF measurements were done in TNO as well as the evaluation and comparison with the simulated values. This correlation makes the conception of the demonstrator substrate with the complete phase shifter structure more promising. This investigation shall give the opportunity to design components, lines and assembling features, which may meet the requested values after manufacturing. The modelling of such a complex system made of unknown material combinations and geometries need to be adapted by the use of different coefficients. The test parts of the 3rd run with '2118_2, including high-k-tape or 40µm-Tape are in table 1.

nr.	board	cap. built by	general appearance
21	DuPont 951 + Au	DP 951 C2	very smooth top surface
22	DuPont 951 + Au	DP 951 C2	very smooth top surface
23	DuPont 951 + Au	2 x ESL 41210, 2nd is perforated too	very smooth top surface. a little larger than 21, 22
24	DuPont 951 + Au	1 x ESL 41210	substantial warping, not applicable
25	ESL 41110 + Au	2 x ESL 41210 2nd is solid	substantial warping, not applicable
26	ESL 41110 + Au	ESL 41210, 2nd is perforated too	Flat top surface, little warping; only on the edge of TRL

table 1: description of test boards ##21..26

The measurements done in TNO took place at different frequencies and with different types of probes. A vector network analyser (45 MHz -50 GHz) HP8510C has been used and measurements up to 20 GHz have been made. As an example the measurements at transmission lines of the samples 21.. are listed in table 2.

board nr.	layer #	Z0 [Ω]	α [dB/mm]	ε_{eff}	tan δ
21	2	40.5	0.013	6.05	0.012
22	2+1	44.5	0.015	5.45	0.015
23	2+1	44.1	0.005	8.47	0.003
26	2	53.7	0.012	3.62	0.019

table 2: measured values on boards ##21-23, 26

It illustrates the strong influence of the base material and the inserted 41210 layer. Summarizing the main result of all these test runs is knowledge in:

- the effective k, attenuation, loss
- achievable impedances
- preferences regarding line widths
- revision of design rules
- achievable density etc.

Technological investigation

Additional objectives of investigations were the technological topics: how to process the materials, how to take care that best possible compatibility can be achieved. To learn about the divergence of the parameters of components in a manufacturing lot or the repeatability of equally parts, produced in different lots.

The test layout contains different RF test structures, single components as well as combined features. The typical components shall give an overview, what high frequency relevant properties will be achievable using the chosen material systems. It has been necessary to process the unfamiliar materials and combinations of materials with design rules being even not qualified.

Because LTCC is able to solve a high demand regarding integration of passives surface integrated and embedded in the ceramic substrates the test vehicle has been designed with the opportunity to check and to qualify the integration of RF suitable resistors and capacitors as well as structures, which can achieve special properties regarding loss and characteristic impedance. In cooperation with the material's supplier ESL different capacitance effective pastes and tapes as well as resistor pastes have been tested.

Additionally, out of the RF requirements and the miniaturization request the building of cavities for mounting the RF switches in, are in the focus of the machining development. The openings for the chips should be equally formed, because the gap between chip and LTCC has to be tight, but not too close to avoid mounting problems. A high reliable process for hole formation has to fit to the screen printing patterns close to the opening.

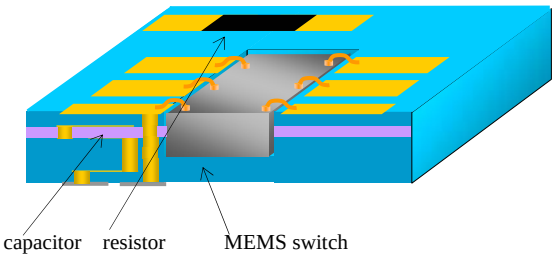

Fig. 11: principle of phase shifter substrate with cavity for short and low inductance wire bonds

Summary and conclusions

All the boards had shown the targetted effect of higher capacitance. Several capacitors had a resonance frequency close to the work frequency, but this is partially a design issue and can be solved.

Partial incompatibilities could be minimized or compensated by different techniques. Less successful control mechanisms have not been tracked.

RF behaviour, measured on the test boards makes promising for the properties of the real phase shifter demonstrator to be manufactured in the next weeks.

The use of the high-k (or thin) layers to realize capacitors with a certain C value with reduced size and thus lower inductance is practical. Higher capacitance values are obtained with the high-k ESL layer: up to 40 pF. But this requires also special presented processing guidelines.

A recalculation in the simulation software as well as the design work for such substrates can base now on the values out of a quantity of proven samples with these materials.

Future work

Additional work is just ongoing to verify the method to combine the via punched and filled high-k-tape with the other tapes (tape 1 has electrodes on the bottom side too in this case) is being investigated regarding mechanical behaviour right now. It is recommended to know more about, how other functional elements behave while they are folded during the lamination / compression / sintering process to get an homogeneous stack over and around the capacitive tape “islands”.

This 2nd structured 41210 layer before the lowest layer gives the advantage of lowest warping (uncritical), but double the local difference in substrate thickness too. This is primarily when the lamination of the tapes is carried out isostatically. Some additional investigation and process optimisation need to be done to use these techniques.

Acknowledgements

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